Amendments to the Claims:

This listing of claims will replace all prior versions, and listings of claims in the application:

Listing of Claims:

Claim 1. (Previously presented) An integrated circuit comprising:

a control block comprising:

a first series of delay elements including a first delay element coupled to receive a reference clock input, each delay element having an input;

a first selection circuit coupled to a plurality of inputs of the first series of delay elements;

a phase detector having a first input coupled to the reference clock input and a second input coupled to an output of the selection circuit; and

a counter coupled to an output of the phase detector and having an output coupled to a control input of each element in the series of delay elements;

an input buffer;

a second series of delay elements including a second delay element coupled to receive an output of the input buffer, each delay element having an input; and

a first register having a clock input coupled to an output of the second series of delay elements.

Claim 2. (Original) The integrated circuit of claim 1 wherein the first selection circuit comprises a multiplexer.

Claim 3. (Previously presented) The integrated circuit of claim 1 further comprising:

a second selection circuit coupled to a plurality of inputs of the second series of delay elements and having an output coupled to the clock input of the first register.

Claim 4. (Previously presented) The integrated circuit of claim 3 wherein the first and second selection circuits each comprise a multiplexer.

Claim 5. (Previously presented) The integrated circuit of claim 3 wherein the first register is a flip-flop.

Claim 6. (Previously presented) The integrated circuit of claim 3 wherein the first register comprises a first flip-flop and a second flip-flop, and an output of the second selection circuit couples to a clock input of a the first flip-flop and a complementary clock input of the second flip-flop.

Claim 7. (Original) The integrated circuit of claim 6 wherein the first and second flip-flops are coupled to a data input.

Claim 8. (Original) The integrated circuit of claim 3 wherein the integrated circuit is a field programmable gate array.

Claim 9. (Previously presented) An integrated circuit comprising:

a control circuit to receive a reference clock and provide a plurality of control bits; and

a first delay line to receive the plurality of stored control bits wherein the first delay line comprises:

a first series of delay elements each having an input; and

a first select circuit coupled to a plurality of inputs of the first series of delay elements;

wherein the control circuit comprises a second delay line to receive the plurality of stored control bits wherein the second delay line comprises:

a second series of delay elements each having an input;

a second select circuit coupled to a plurality of inputs of the second series of delay elements; and

a phase detector having a first input coupled to an input of the second series of delay elements and a second input coupled to an output of the second select circuit.

Claim 10. (Previously presented) The integrated circuit of claim 9 wherein the first select circuit is a multiplexer.

Claim 11. (Previously presented) The integrated circuit of claim 9 wherein the first and second select circuits each comprise a multiplexer.

Claim 12. (Previously presented) The integrated circuit of claim 11 wherein the control circuit further comprises:

a counter to receive the phase detector output and provide the control bits.

Claim 13. (Original) The integrated circuit of claim 12 wherein a polarity of the phase detector output depends on the relative phase of the reference clock and the output of second select circuit, and the counter is an up-down counter that counts up when the phase detector output has a first polarity, and counts down when the phase detector output has a second polarity.

Claim 14. (Previously presented) The integrated circuit of claim 11 wherein the first series of delay elements is to delay a read strobe signal.

Claim 15. (Previously presented) The integrated circuit of claim 14 further comprising a storage element to receive an output of the first select circuit.

Claim 16. (Previously presented) The integrated circuit of claim 9 wherein the control circuit is a delay-locked loop.

Claim 17. (Previously presented) The integrated circuit of claim 9 wherein the integrated circuit is a field programmable gate array.

Claim 18. (Currently amended) A method of delaying a data strobe signal comprising:

receiving a reference clock signal;

delaying the reference clock signal using a first number of delay elements, each delay element providing a delayed reference clock signal;

selecting one of the delayed reference clock signals;

comparing the phase of the reference clock signal to the phase of the selected delayed reference clock signal to generate the plurality of control signals, the control signals coupled to the first number of delay elements and a second number of delay elements; ~~and~~

delaying the data strobe signal using ~~a~~ the second number of delay elements, wherein each of the second number of delay elements provide a delayed strobe signal;

selecting one of the delayed strobe signals; and

receiving a data signal using the selected one of the delayed strobe signals.

Claims 19-20. (Cancelled)